UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/605,405	09/29/2003	Seetharam Gundurao	BUR920020053US1	2404

31647 7590 03/06/2007

DUGAN & DUGAN, P.C.
55 SOUTH BROADWAY
TARRYTOWN, NY 10591

EXAMINER	
TRAN, KHANH C	
ART UNIT	PAPER NUMBER
2611	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	03/06/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/605,405	GUNDURAO ET AL.	
	Examiner	Art Unit	
	Khanh Tran	2611	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 September 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *8,9,11-16,18 and 19* is/are allowed.

6)☒ Claim(s) *1-3,6,7 and 20* is/are rejected.

7)☒ Claim(s) *4,5,10 and 17* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *23 September 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

1. Claim 10 is objected to because of the following informalities: in line 13 "second" should be changed to -- first --; in line 14 "first" should be changed to -- second --. Appropriate correction is required.

2. Claim 17 is objected to because of the following informalities: in line 16 "second" should be changed to -- first --; in line 17 "first" should be changed to -- second --. Appropriate correction is required.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-3, 6-7 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Haq et al. U.S. Patent 7,123,660 in view of Asada et al. U.S. Patent 5,745,533.

Regarding claim 1, in column 5 lines 15-30, see also FIG. 1, Haq et al. teaches a point-to-point connection between two devices, a Jazio receiver 100 on the receiving

device and a Jazio transmitter (not shown) on the transmitter device. In column 6 lines 37-50, Haq et al. teachings can be extended to multiple channels in which a single pair of complementary VTR signals is utilized for every sixteen data input signals. In column 3 lines 25-40, Haq et al. further teaches a programmable delay circuit is coupled to each channel to skew the signals on that channel. The delay value in the programmable delay circuit is based on the alignment of a data input signal relative to a pair of complementary VTR signals.

Haq et al. does not explicitly disclose the Jazio transmitter located in a first clock domain and the Jazio receiver 100 located in a second clock domain.

Nevetheless, further in column 2 lines 55-65, because Haq et al. further suggests that embodiments are also capable of being used in a wide variety of applications, including but not limited to individual or combined use in memories, chipsets, central processing units ("CPUs") network and other processors and controllers, CPU front side, memory, interchip and other buses, peripheral cables and other interconnects, and application specific integrated circuit ("ASIC") devices, it would have been obvious for one of ordinary skill in the art at the time the invention was made that Haq et al. Jazio transmitter and Jazio receiver 100 can be modified to be included in different clock domains.

Haq et al., however, does not expressly disclose the programmable delay selectively adds delay via the programmable delay element as set forth in the application claim.

Asada et al. invention is directed to an apparatus for adjusting a propagation delay time of a timing signal for use in a digital circuit. In column 10 line 60 via column 11 line 20, Asada et al. teaches in FIG. 4 a VDL 48 is a programmable delay circuit capable of changing the signal delay time generated between its input terminal and its output terminal by an input of a digital code. VDL 48 comprises six serially connected inverters 53-1 through 53-6 and a multiplexer 54 receiving as its four input signals a raw input into VDL 48 and respective outputs from three inverters 53-2, 53-4 and 53-6. Multiplexer 54 selects any one of the four input signals received at its input ports M1, M2, M3 and M4, dependent upon an input of a 2-bit control signal for an output as an output signal of VDL 48. A propagation delay time generated upon selecting input port M3 is equivalent to a sum of respective propagation delay times caused by inverters 53-1 and 53-2 and multiplexer 54.

Haq et al. and Asada et al. teachings apply in the same field of endeavor. As disclosed in column 9 lines 50-60, because Haq et al. suggests that the optimum amount of delay for each channel can be determined by varying the skew of the data input signals, one of ordinary skill in the art at the time the invention was made would have been motivated to implement the programmable circuit as taught in Asada et al. invention since the programmable circuit, as taught in Asada et al. invention, has more flexibility to control the amount of signal delay by selecting any stage of the delay chain as recited above.

Regarding claim 2, as recited in claim 1 rejection, Haq et al. teaches a programmable delay circuit is coupled to each channel to skew the signals on that channel.

Regarding claim 3, as shown in FIG. 4 of Asada et al. teachings, the programmable delay circuit VDL 48 comprises six serially connected inverters 53-1 through 53-6 and a multiplexer 54. As common knowledge of one of ordinary skill in the art, inverter can be implemented by a flip-flop, which is a latch.

Regarding claim 6, in column 11 lines 35-45, Haq et al. teaches that in one embodiment, the alignment monitor of receiver group 1003 includes a test monitor 701 shown in FIG. 7A for determining the amount of delay necessary for proper alignment. Each data input signal has a corresponding VTR select register in receiver group 1003 for selecting the VTR signal pair best aligned with it. The foregoing disclosure corresponds to the claimed step of testing operation of the first and second receivers as set forth in the application claim and the claimed step of determining one or more delays as set forth in the application claim. As further recited in claim 1 rejection above, Haq et al. suggests that the optimum amount of delay for each channel can be determined by varying the skew of the data input signals.

The amount of delay necessary for proper alignment, as recited above, is used for the alignment

Regarding claim 7, in column 3 lines 25-35, Haq et al. further teaches that the delay value in the programmable delay circuit is based on the alignment of a data input signal relative to a pair of complementary VTR signals. The delay value may be determined during start-up or during normal operation using an alignment monitor circuit. In view of that, the steps of determining optimum delay can be implemented automatically as appreciated by a person of ordinary skill in the art.

Regarding claim 20, claim is rejected on the same ground as for claim 6 because of similar scope. Furthermore, although Haq et al. and Asada et al. do not teach a computer product as set forth in the application claim, nevertheless, one of ordinary in the art at the time the invention was made would have recognized that the steps performed can be easily implemented on a computer medium with the advance of computer programming.

Allowable Subject Matter

4. Claims 4-5 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

5. Claims 8-9 are allowed.

The following is a statement of reasons for the indication of allowable subject matter:

Regarding claim 8, claim is allowable over prior art of record because Haq et al. and Asada et al. do not disclose a bi-directional system for de-skewing signals on parallel bus channels.

6. Claims 10-16 are allowed.

The following is a statement of reasons for the indication of allowable subject matter:

Regarding claim 10, claim is allowable over prior art of record because Haq et al. and Asada et al. do not disclose an apparatus for use with asynchronous interface as set forth in the application claim.

7. Claims 17-19 are allowed.

The following is a statement of reasons for the indication of allowable subject matter:

Regarding claim 17, claim is allowable over prior art of record because Haq et al. and Asada et al. do not disclose an apparatus comprising a supplemental asynchronous interface device as set forth in the application claim.

Conclusion

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Saito U.S. Patent 6,813,724 B2 discloses "Phase-Controlled Source Synchronous Interface Circuit".

Miller et al. U.S. Patent 5,712,883 discloses "Clock Signal Distribution System".

Lo et al. U.S. Patent 5,970,052 discloses "Method For Dynamic Testing".

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Khanh Tran whose telephone number is 571-272-3007. The examiner can normally be reached on Monday - Friday from 08:00 AM - 05:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jay Patel can be reached on 571-272-2988. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

KCT

Khanh Cong Tran

03/02/2007
Khanh Tran
Primary Examiner, AU 2611